Abstract

A dual loop (PLL/DLL) data synchronization system and method for plesiochronous systems is provided. A dual loop data serializer includes a phase lock loop (PLL) and a delayed lock loop (DLL) configured with a phase shifter in the feedback path of the PLL. The dual loop serializer locks to the input of the DLL instead of the local reference. Thus, the DLL adjusts the frequency from the PLL so that it matches the desired data rate. Each loop may be optimized for jitter tolerance with the net effect generating a synthesized clean clock (due to narrow bandwidth filtering) and VCO noise suppression (due to wide bandwidth filtering). A dual loop retimer includes a dual loop serializer (PLL/DLL) and a clock recovery DLL. The retimer resets the jitter budget to meet transmission requirements for an infinite number of repeater stages.